

PG401 A02

4GB GDDR5, 256b, 128Mx32

Tall DVI-I + DP + DP + DP/HDMI + DP

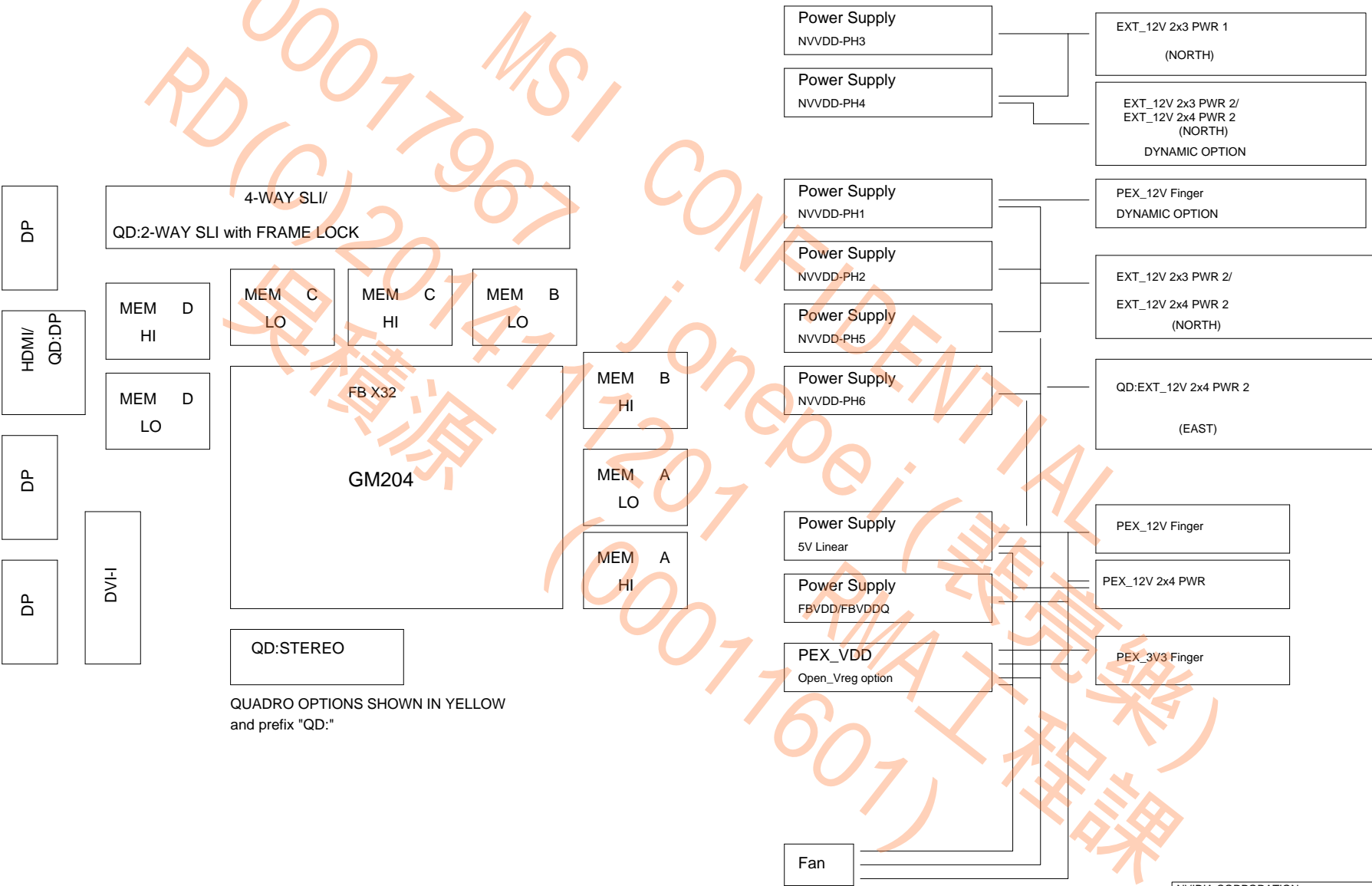
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QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

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ASSEMBLY	BASIC LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	Block Diagram

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PCI Express

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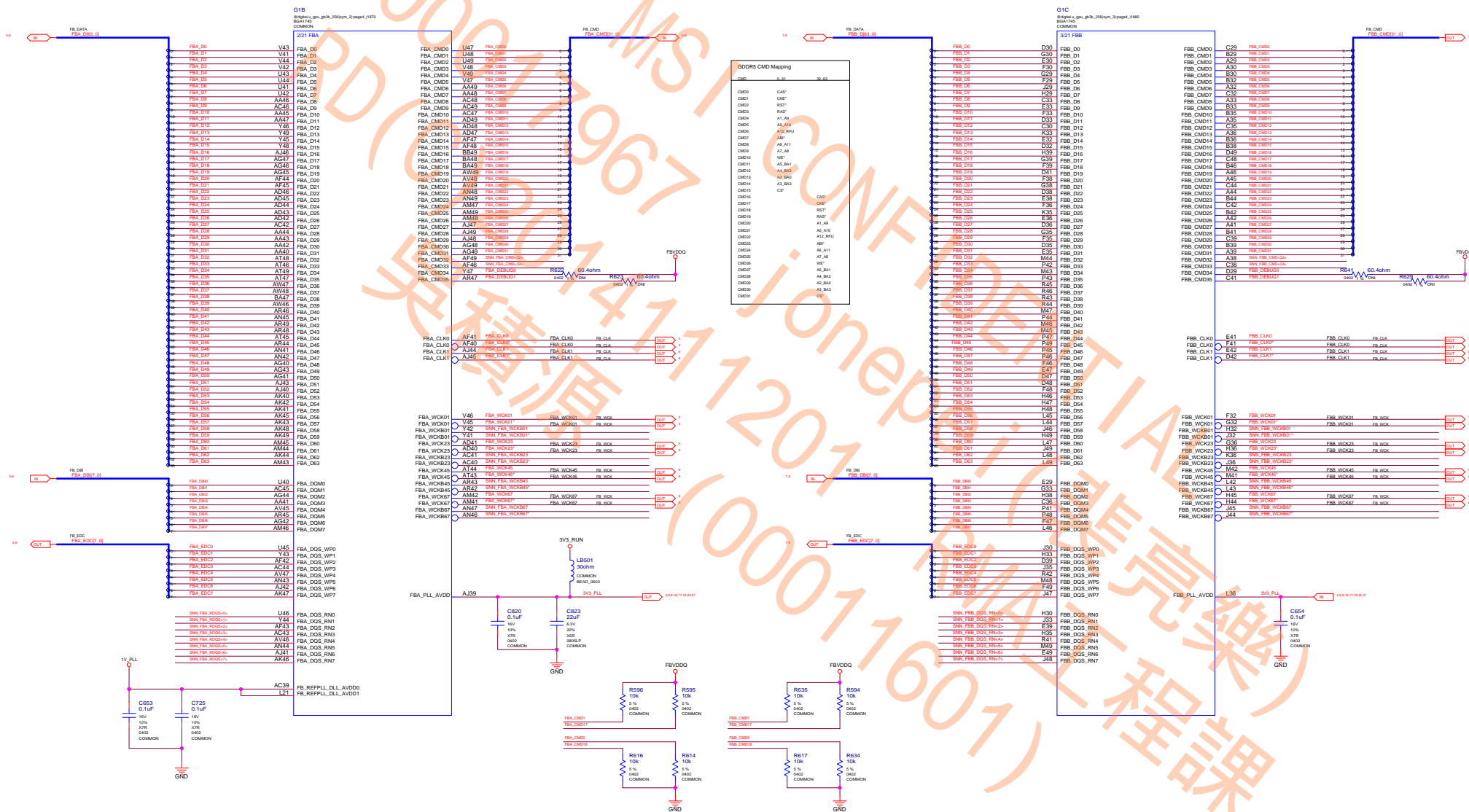
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ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL MEMORY GPU Partition A/B

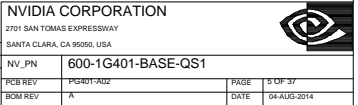
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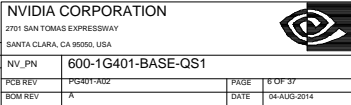
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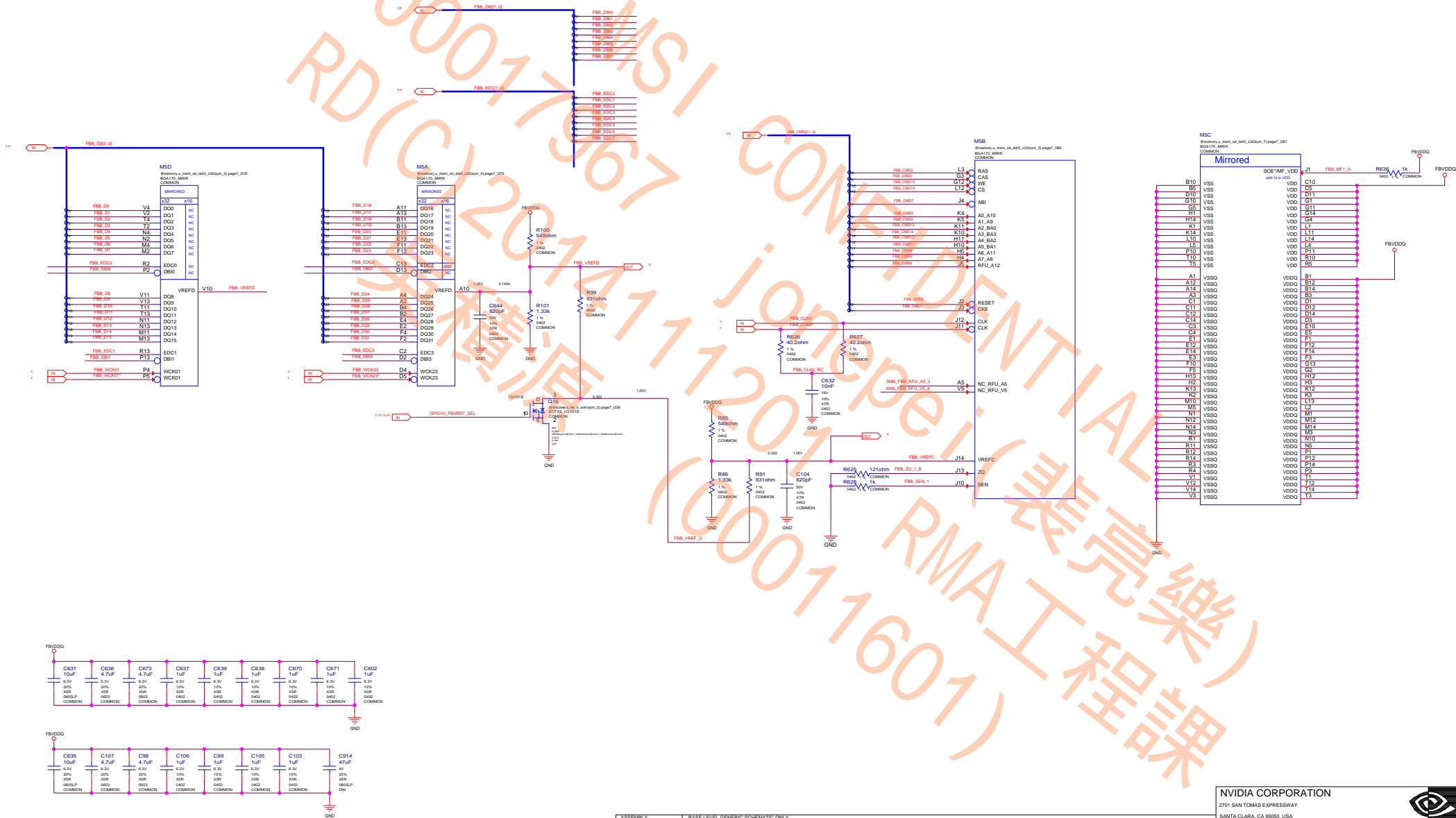
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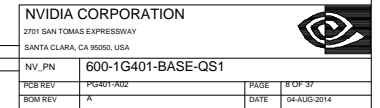




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ASSEMBLY
PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBB[31:0]

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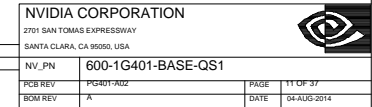
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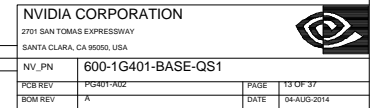
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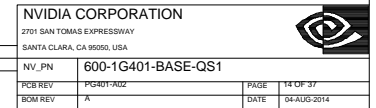
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PAGE DETAIL	GPU PWR and GND

Based on GB2-X GDDR5 FBVDDQ Decap Guideline



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PAGE DETAIL	GPU Decoupling


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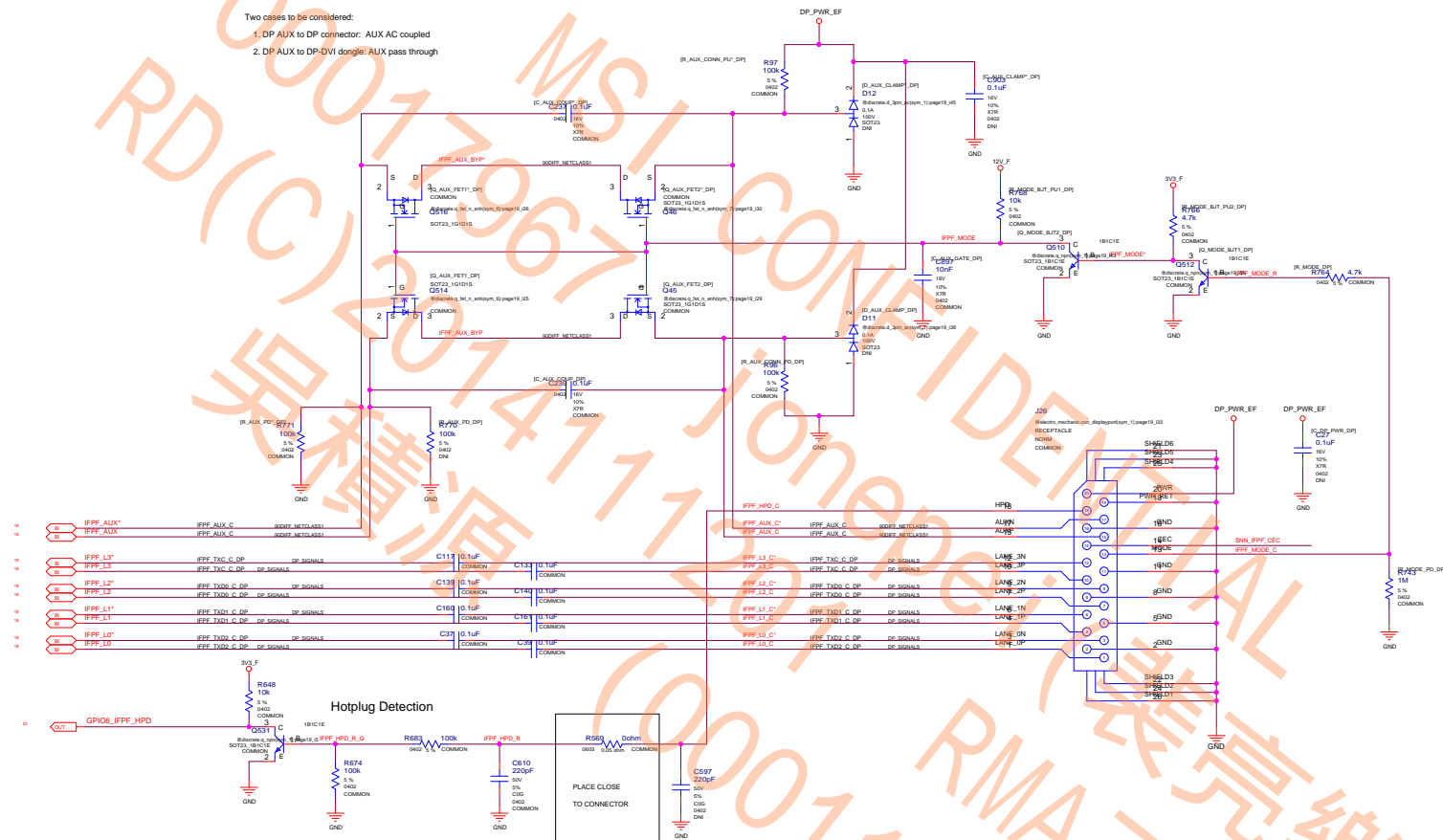
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL	IFPF DP

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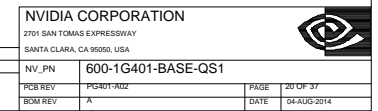
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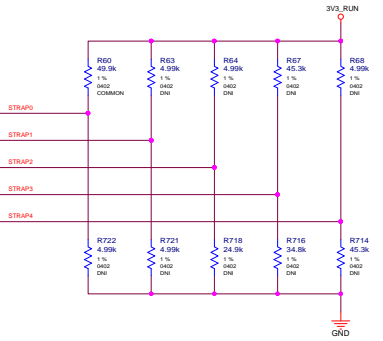
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KEPLER			
STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Overlap*
STRAP2	PCI_DEVID [3:0]*	0100 - (0x1184)*	25K PD 425 GP1U*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*
	PEX_MAX_SPEED*	1*	FOR GEN2/3*
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*
	*		

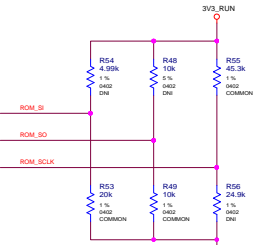
ROM_SI	RAMCFG[0]*	1*	
	RAMCFG[1]*	1*	0111 for 64Mx32 256-bit SAMSUNG SAMSUNG for SKI-D primary memory
	RAMCFG[2]*	1*	45K PD*
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30K PD*
	FB[0]_APERTURE_SIZE*	1*	For 128MB*
	FB[1]_APERTURE_SIZE*	0*	For 128MB*
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*
	PCI_DEVID_EXT[5]*	0*	For 0x1184*
	SUB_VENDOR*	1*	Dedicated BIOS*
	PCI_DEVID_EXT[4]*	0*	For 0x1184*

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2K 1% TO GND



MAXWELL			
GC6	SEE TABLE BELOW		
RAMCFG	RAMCFG[0]*	1*	
	RAMCFG[1]*	1*	20K PD*
	RAMCFG[2]*	0*	
	RAMCFG[3]*	0*	
VGA_DEVICE	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	10K PD*
	PCIE_CFG*	0*	
	DEVID_SEL*	0*	
SOR	SOR0_EXPOSED*	1*	
	SOR1_EXPOSED*	1*	45K PU*
	SOR2_EXPOSED*	1*	
	SOR3_EXPOSED*	1*	

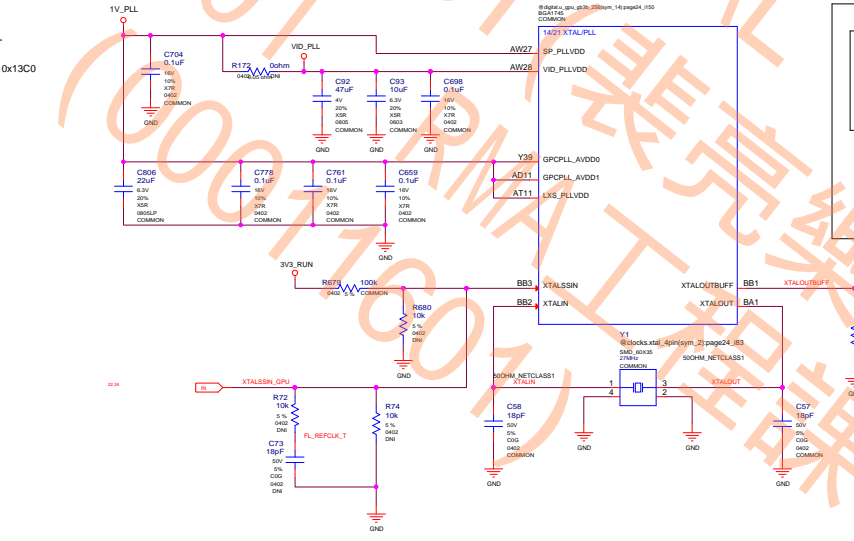
MAXWELL		
STRAP0	3.3V	1.85V
STRAP1	1.85V	0V
STRAP2	0V	0V
STRAP3	0V	0V
STRAP4	0V	0V




	GND	3V3
5K	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	32Mx32 256-bit Elpida		
0010	32Mx32 256-bit Hynix		
0011	32Mx32 256-bit Samsung		
0100	Reserved		
0101	64Mx32 256-bit Elpida		
0110	64Mx32 256-bit Hynix		
0111	64Mx32 256-bit Samsung		
1000	Reserved		
1001	32Mx32 192-bit Elpida		
1010	32Mx32 192-bit Hynix		
1011	32Mx32 192-bit Samsung		
1100	Reserved		
1101	64Mx32 192-bit Elpida		
1110	64Mx32 192-bit Hynix		
1111	64Mx32 192-bit Samsung		

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	128Mx32 256-bit Elpida		
0010	128Mx32 256-bit Hynix		
0011	128Mx32 256-bit Samsung		
0100	Reserved		
0101	64Mx32 256-bit Elpida		
0110	64Mx32 256-bit Hynix		
0111	64Mx32 256-bit Samsung		



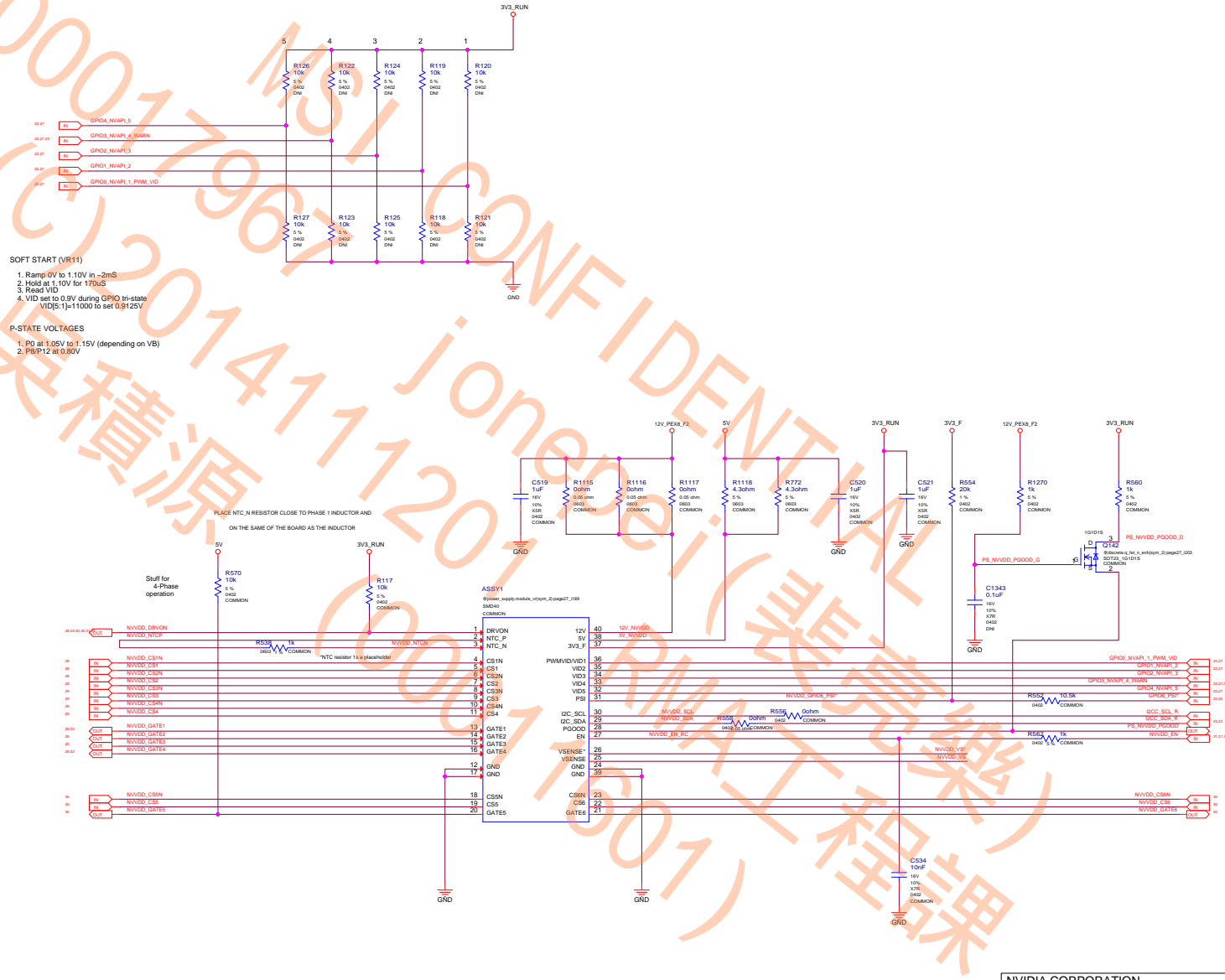


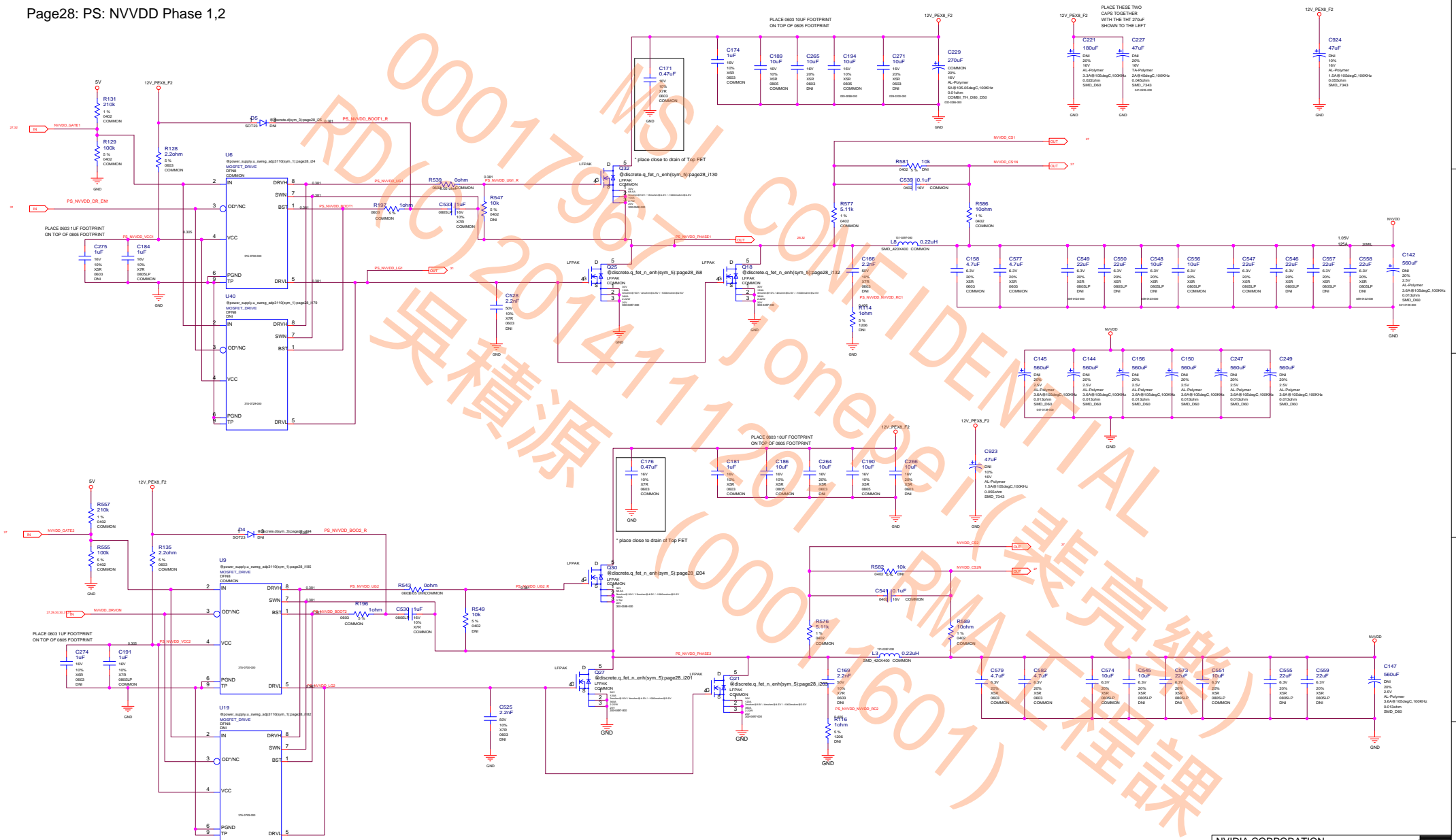
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VID Table

GPIO4 VID_5	GPIO3 VID_4	GPIO2 VID_3	GPIO1 VID_2	GPIO0 VID_1	VOUT
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V





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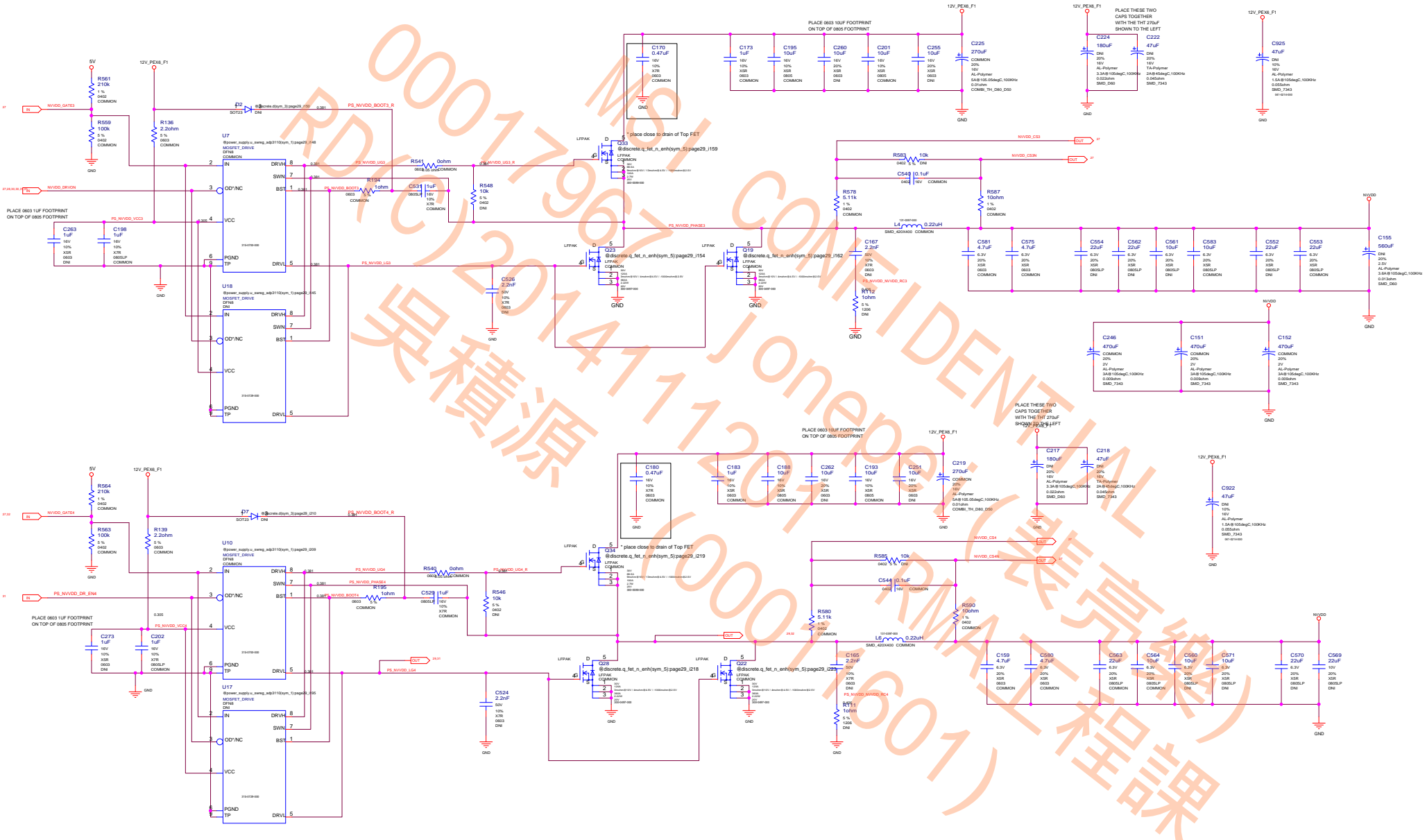
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVDD Phase 1,2

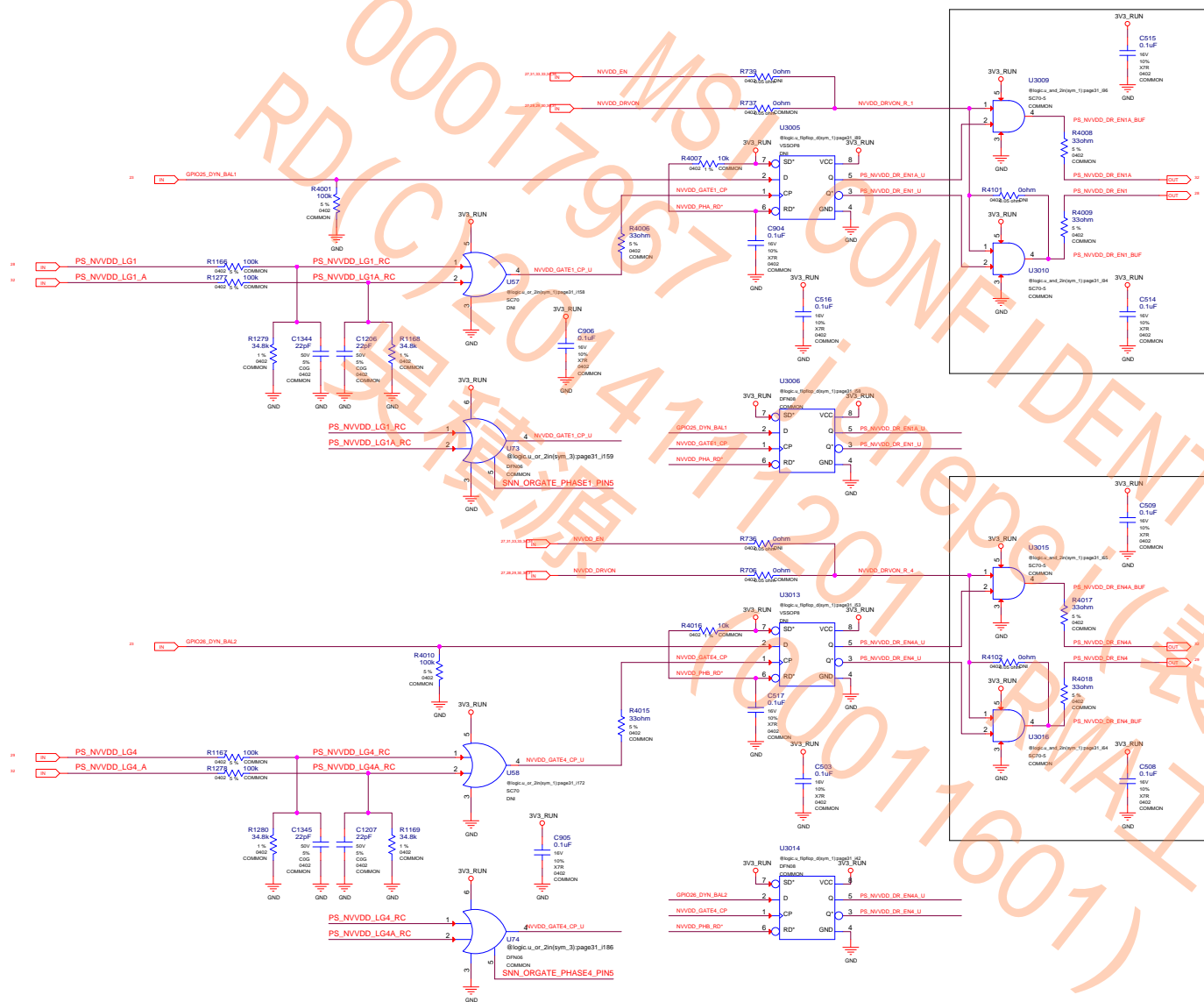
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Dynamic Power Balance Logic

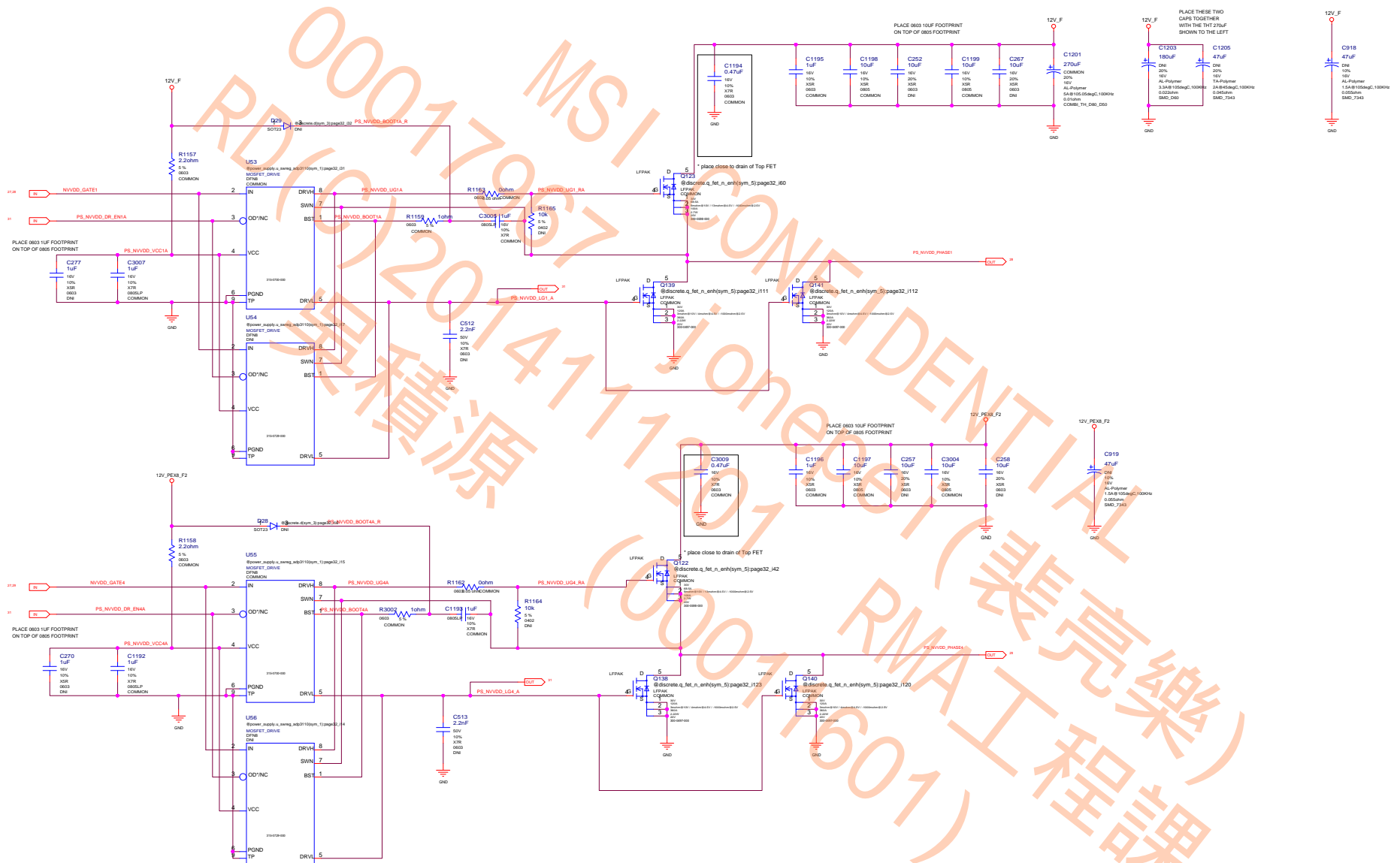
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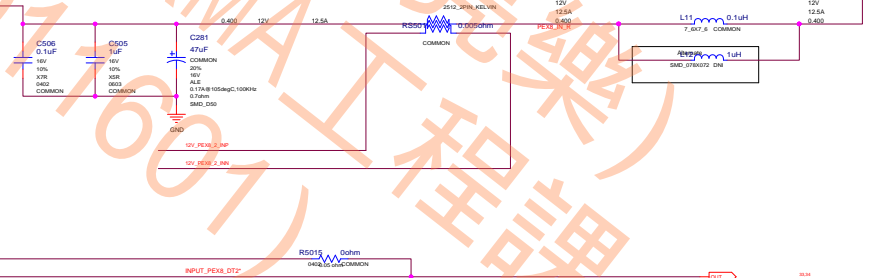
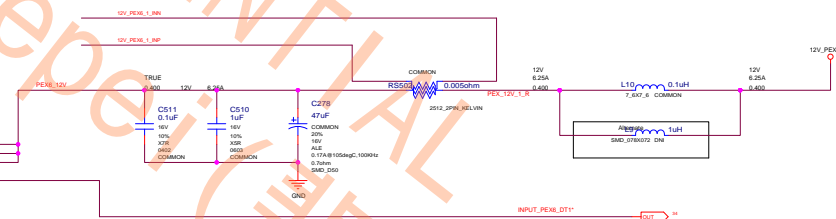
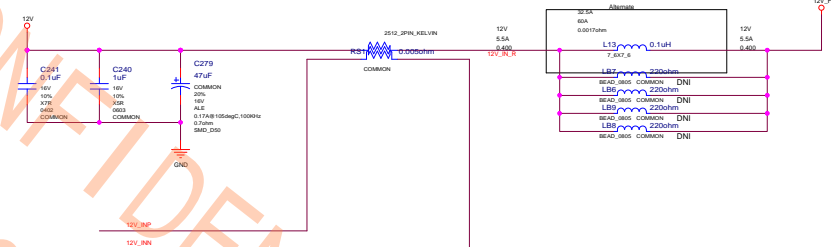
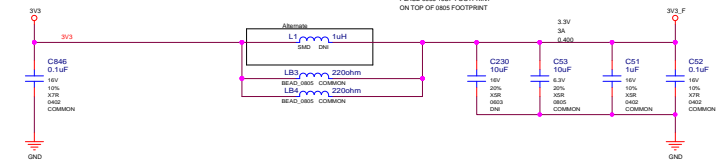
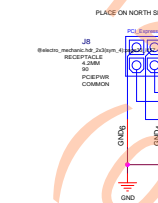
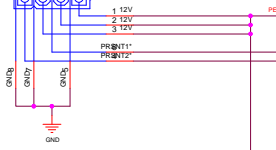
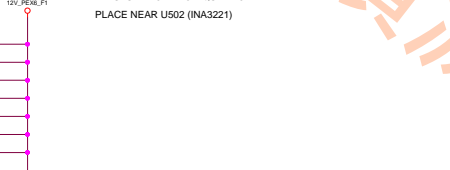
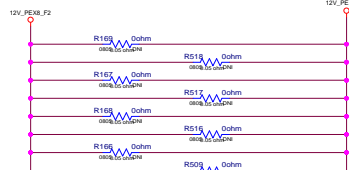
NV_PN	600-1G401-BASE-QS1
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Dynamic Power Balance Phases

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NV_PN		600-1G401-BASE-QS1	
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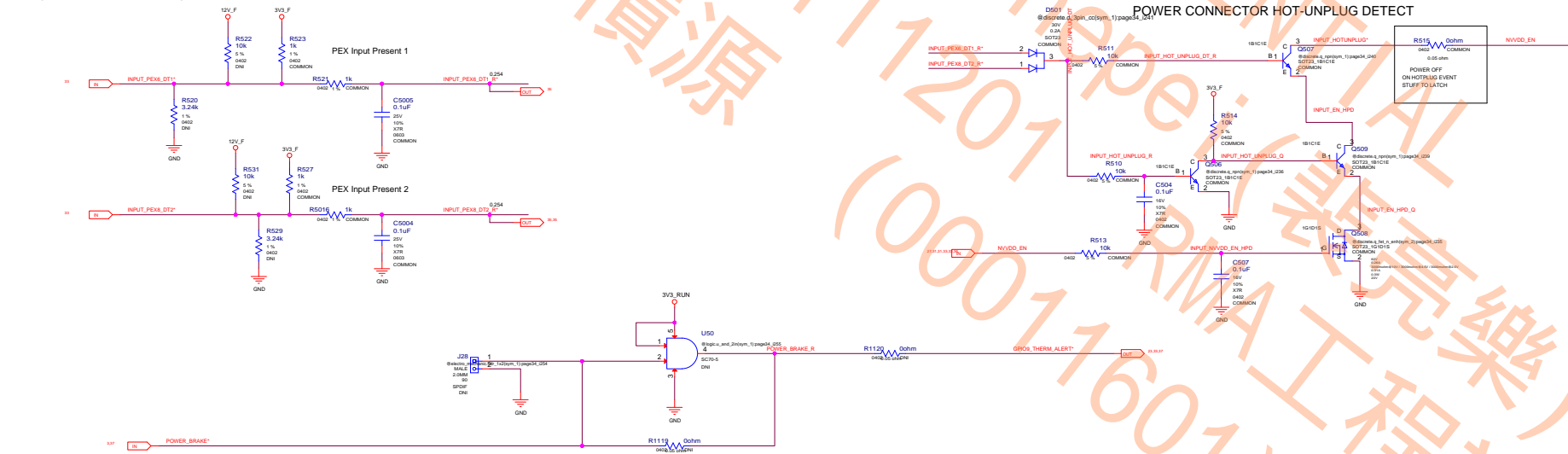
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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THERM OVERT SHUTDOWN LATCH

IFP_IOVDD (backdrive prevention)

PEX Input - NVVDD Power Sequence

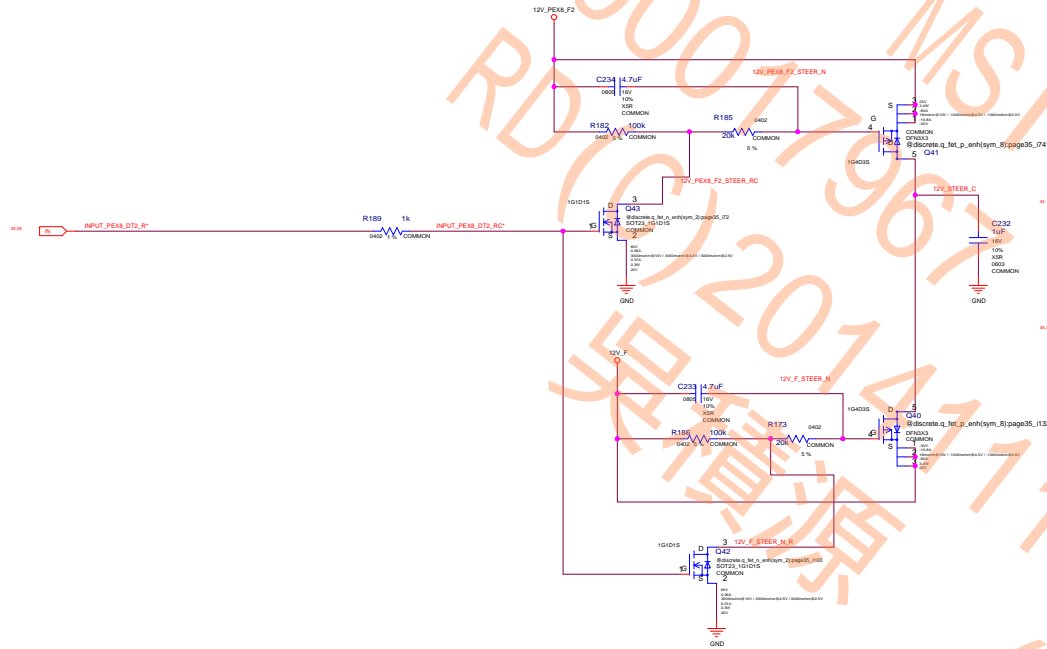


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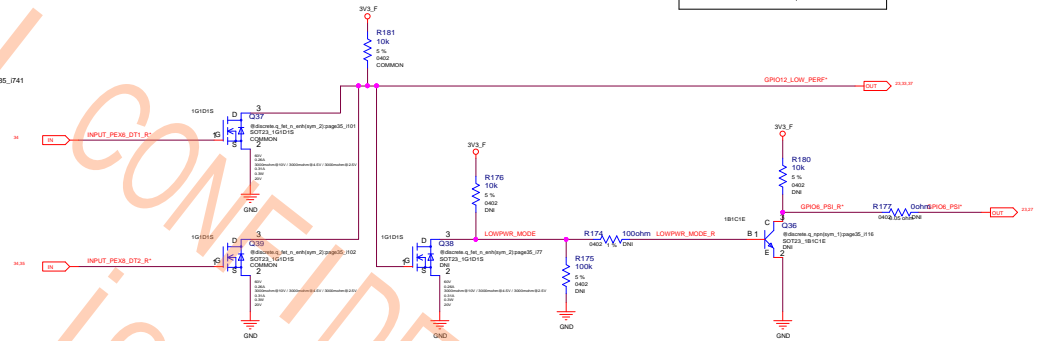
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Shutdown

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PEX Input - 12V Current Steering FETs

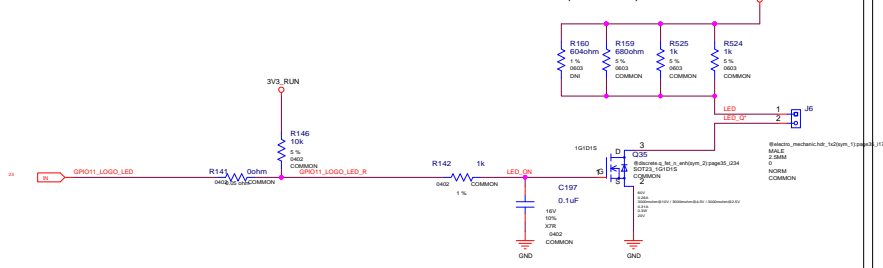


PEX Input - Power Level/PSI* Control

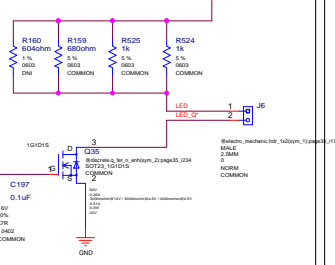


GPO12_LOW_PERR*	GPU SPEED
0	Slow
1	Normal

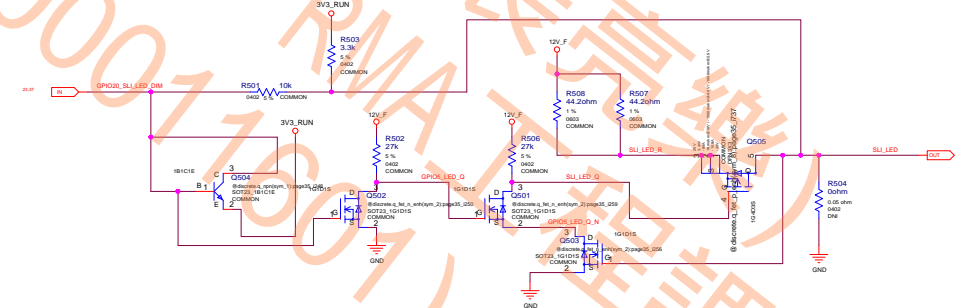
GeForce Logo LED



LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)



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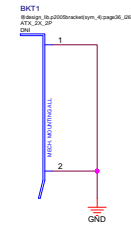
BOX REV A

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ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL PS: 12V Current Steering PSB Control and LED

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Brackets:



Bracket Screw

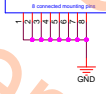


BGA SOCKET ASSY

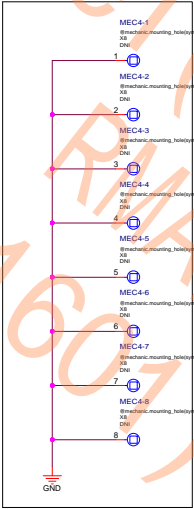
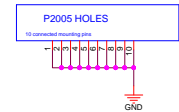


GPU Stiffner

BOARD STIFFENER



Mechanical Holes Symbol



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MECH Bracket/Thermal

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